IN THE CLAIMS

Please cancel claims 1 - 20.

Please enter the following new claims 21 - 37:

21. (New) A pull-up element for a silicon based semiconductor circuit comprising:

a silicon based n-channel metal insulator semiconductor (MIS) field effect transistor (FET) configured to include a trapping region situated proximate to an interface with a channel of said silicon based MISFET, said channel coupling a high voltage potential supplied to the silicon based semiconductor circuit and a first node of the silicon based semiconductor circuit;

said trapping region including carrier trapping sites configured for trapping and de-trapping charge carriers from said channel;

wherein said trapping sites are characterized by an energy level that is higher than a conduction band edge of said channel and lower than a conduction band of said trapping region;

said trapping sites further having a concentration and arrangement so that said channel can be controlled and shut off by operation of said trapping region to reduce static power dissipation by the pull-up element during operation of the silicon based semiconductor circuit.

22. (New) The pull-up element of claim 21, wherein said trap energy level is set so that said trapping sites trap primarily hot carriers flowing in said channel.

23. (New) The pull-up element of claim 21, wherein the circuit is a static random access memory (SRAM) cell and said first node is a storage node for storing a voltage representing a data value.

24. (New) The pull-up element of claim 23, wherein said pull-up element is turned off during a period when the memory cell is storing data.

25. (New) The pull-up element of claim 21, wherein the circuit is a logic circuit.

26. (New) The pull-up element of claim 21, wherein said trap energy level is set to approximately .5 eV higher than said conduction band edge of said channel.

27. (New) The pull-up element of claim 21, wherein said silicon based MISFET exhibits a negative differential resistance characteristic in said channel.

28. (New) The pull-up element of claim 21 wherein said trapping region is contained within an dielectric layer positioned between said channel and a control gate for the silicon based MISFET.

29. (New) The pull-up element of claim 21, wherein the pull-up element includes at least one source/drain region that is shared with another MISFET within the semiconductor based circuit.

30. (New) The pull-up element of claim 21, further including a p-type dopant distributed in said channel so as to increase an electrical field strength and enhance said trapping of said carriers.

31. (New) The pull-up element of claim 21, wherein the silicon based semiconductor circuit includes other MISFETs which share a common channel type as said silicon based MISFET, such that only a single channel dopant type is used in the silicon based semiconductor circuit.

32. (New) A pull up element for a silicon-on-insulator (SOI) logic circuit which includes a field effect transistor comprising:

a silicon based n-channel metal insulator semiconductor (MIS) field effect transistor (FET) configured to include a trapping region situated proximate to an interface with a channel of said silicon based MISFET, said channel coupling a high voltage potential supplied to the silicon based semiconductor circuit and a first node of the SOI logic circuit;

said trapping region including carrier trapping sites configured for trapping and de-trapping charge carriers from said channel;

wherein said trapping sites are characterized by an energy level that is higher than a conduction band edge of said channel and lower than a conduction band of said trapping region;

said trapping sites further having a concentration and arrangement so that said channel can be controlled and shut off by operation of said trapping region to reduce static power dissipation by the pull-up element during operation of the SOI logic circuit.;

wherein the silicon based n-channel MISFET and the field effect transistor share at least one common gate insulation layer.

33. (New) The pull up element of claim 32, wherein a channel region of the silicon based n-channel MISFET and a channel region of the field effect transistor include a common channel type dopant.

34. (New) The pull up element of claim 32, wherein said silicon based n-channel MISFET includes a negative differential resistance operating region which is not based on band-to-band tunneling.

35. (New) A pull up element for a CMOS based logic circuit comprising:

a silicon based n-channel metal insulator semiconductor (MIS) field effect transistor (FET) configured to include a trapping region situated proximate to an interface with a channel of said silicon based MISFET, said channel coupling a high voltage potential supplied to the silicon based semiconductor circuit and a first node of the CMOS based logic circuit;

said trapping region including carrier trapping sites configured for trapping and de-trapping charge carriers from said channel, and said trapping sites are characterized by an energy level that is higher than a conduction band edge of said channel and lower than a conduction band of said trapping region;

said silicon based n-channel MISFET including an independent control gate which can be switched off during selected periods to reduce standby current of the CMOS based logic circuit.

36. (New) The pull up element of claim 35, wherein said silicon based n-channel MISFET and an access transistor of the CMOS based logic circuit are formed with at least one common gate insulation layer and one common source/drain region.

37. (New) The pull up element of claim 35, wherein said silicon based n-channel MISFET includes a negative differential resistance operating region which is not based on band-to-band tunneling.